CLAIMS

What is claimed is:

1. A method of making a flash memory cell including a substrate having a floating gate of a first thickness, the method comprising:

depositing an insulator on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and

polishing the insulator until the second thickness is substantially equal to the first thickness, whereby polishing the insulator produces a floating gate and insulator layer.

2. The method of claim 1, wherein the insulator is a high quality oxide.

3. The method of claim 1, wherein the first thickness is no more than approximately 2000 Å, and the second thickness of the insulator is between approximately 1000 Å and 5000 Å.

4. The method of claim 1, wherein polishing the insulator includes chemical mechanical polishing.

5. The method of claim 1, further comprising:

depositing a dielectric layer on the floating gate and insulator layer;

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

6. The method of claim 5, wherein depositing the dielectric layer includes depositing an ONO layer.

7. A method of making a flash memory cell having a substrate and a tunnel oxide formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide, the floating gate layer having a first thickness;

etching the floating gate layer;

depositing an insulator on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and

polishing the insulator until the second thickness is substantially equal to the first thickness, whereby polishing the insulator produces a floating gate and insulator layer.

8. The method of claim 7, wherein the insulator is a high quality oxide.

9. The method of claim 7, wherein the first thickness is no more than approximately 2000 Å, and the second thickness of the insulator is between approximately 1000 Å and 5000 Å.

10. The method of claim 7, wherein polishing the insulator includes chemical mechanical polishing.

11. The method of claim 7, further comprising:

depositing a dielectric layer on the floating gate and insulator layer;

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

12. The method of claim 11, wherein depositing the dielectric layer includes depositing an ONO layer.

13. The method of claim 7, further comprising, prior to depositing the insulator, thermally oxidizing the floating gate to seal the vertical surfaces of the floating gate.

14. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped polysilicon.

15. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped amorphous silicon.

16. A flash memory cell comprising:

a substrate having a tunnel oxide;

a floating gate disposed on the tunnel oxide, the floating gate having a plurality of vertical surfaces, each vertical surface having a height of a first thickness;

an insulator disposed on the tunnel oxide and abutting the plurality of vertical surfaces of the floating gate;

a dielectric layer disposed on the floating gate; and

a control gate disposed on the dielectric layer, the control gate, the dielectric layer and the floating gate forming a stacked gate structure of the flash memory cell,

wherein the insulator is formed by first depositing a layer of the insulator on the substrate, the insulator covering the floating gate and having a second thickness greater than the first thickness, and then polishing the insulator until the second thickness is approximately equal to the first thickness.

17. The memory cell of claim 16, wherein the insulator is a high quality oxide.

18. The memory cell of claim 16, wherein the first thickness is no more than approximately 2000 Å.

19. The memory cell of claim 18, wherein the second thickness is between approximately 1000 Å and 5000 Å.

20. The memory cell of claim 16, wherein the dielectric layer is an ONO layer.

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